MITEL SEMICONDUCTOR

AN4666

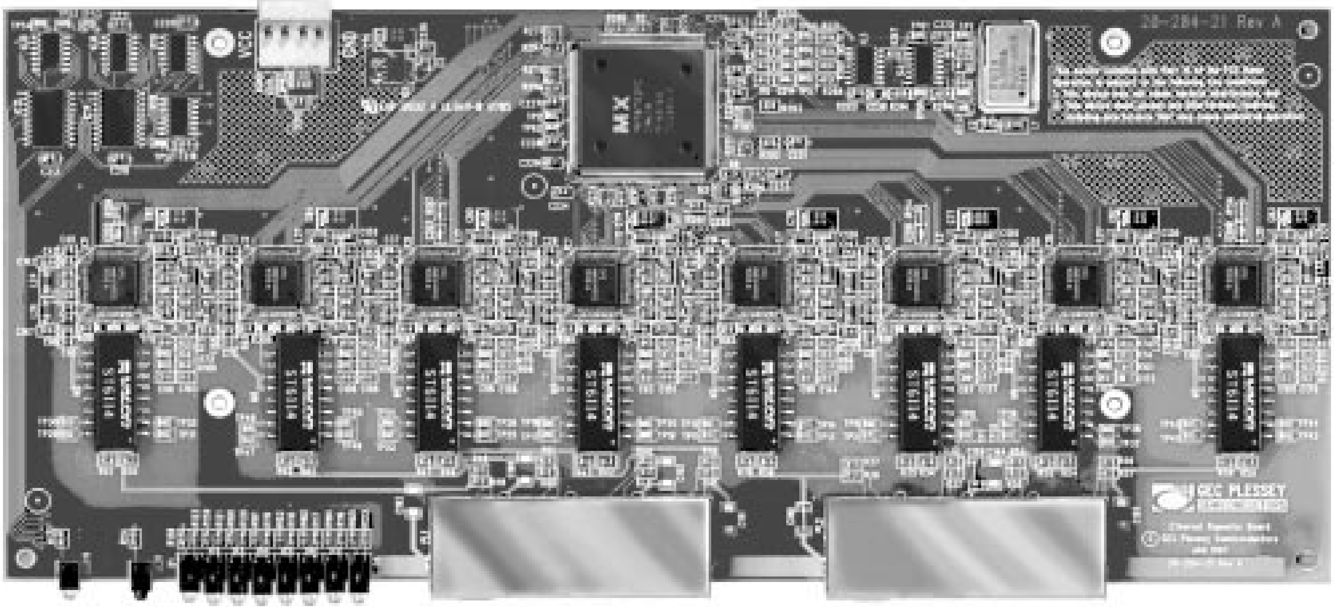
100 Base-TX Symbol Repeater based on the NWK914

Application Note

AN4666 - 1.4 January 1997

1 OVERVIEW

This application note is intended to highlight the design considerations for a 100BASE-TX eight port Symbol based repeater using the Mitel Semiconductor NWK914 and the Macronix MX98741 Repeater Interface Controller (RIC). Topics covered are the system block level, components and layout requirements.



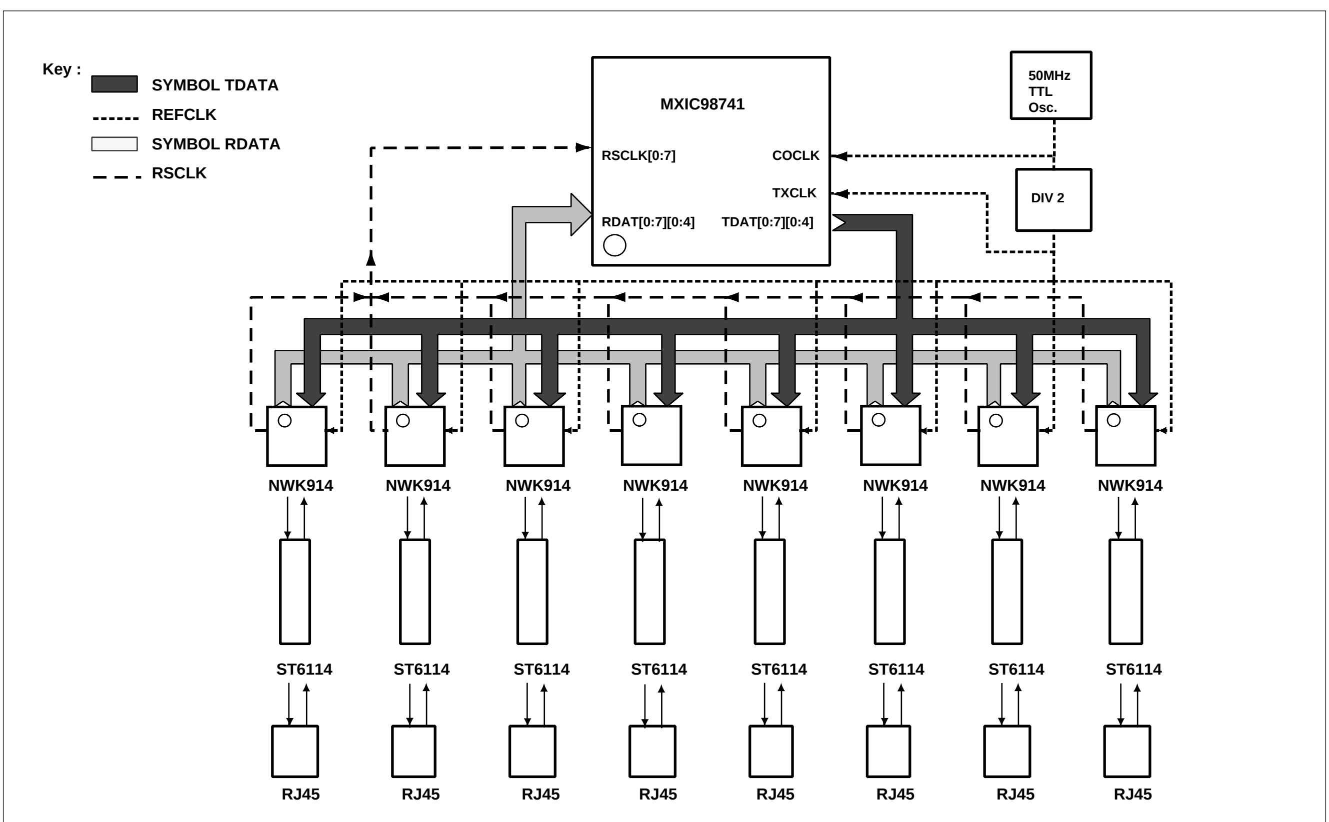


Fig.1 Repeater system overview

2 REPEATER SYSTEM OVERVIEW

This section considers the functional blocks required for a symbol repeater design. The basic requirements are one RJ45, magnetics and NWK914 per port. The NWK914 includes the transceiver with data and clock recovery to the symbol level. The PCS and logic to MII is internal to the MX98741. The MX98741 supports eight symbol physical layer devices. This provides a simple and low cost solution for an eight port repeater with low system level silicon count.

The simplified block diagram is illustrated below, Fig.1.

2.1 Transmit Operation

The NWK914 requires a reference clock, REFCLK, of 25MHz which clocks in the 5 bit transmit data TDAT[0:4]. The MX98741 also requires a transmitter clock TXCLK which is driven by the same 25 MHz crystal controlled clock source. This supplies the reference to the transmit logic of the MX98741. The TDAT[0:7][0:4] is driven off the rising edge of the TXCLK.

2.2 Receive Operation

The NWK914 phase locks to the incoming data to produce a recovered clock at 25MHz - RXC. The NWK914 also recovers the 5 bit data RDAT[0:7][0:4].

The RXC of the NWK914 is fed into the RSCLK pin required by the MX98741 to pace in the recovered symbol data RDAT[0:7][0:4] of the NWK914.

2.3 Clock Distribution and Configuration

The NWK914 only requires two clock connections, R25OUT and REFCLK in this application.

The MX98741 in this application requires eleven clocks TXCLK , RSCLK[0:7], COCLK and REGCLK.

TXCLK and RSCLK[0:7] are described in the above section.

COCLK is the repeater core clock that has to be 50MHz, and REGCLK is the register clock that is used as a reference to display the status of each port and to latch information inside the MX98741 which has to be less than 12.5MHz.

To accommodate the above clocking recommendations the following is the suggested scheme to be implemented. See Fig.2. The SN74F74 is used to divide down the reference clock frequency and the SN74CT2525 is a low skew clock driver to regenerate the reference clocks to the NWK914.

3.0 LAYOUT GUIDELINES

The following section contains recommended layout techniques that should be followed to maximise the performance and functional implementation of the NWK914. The NWK914 provides connectivity from the cable to the symbol interface.

3.1 Cable to NWK914

In this application the cable physical interface is an RJ45 connector socket which is connected to the magnetics which is in turn connected to the NWK914. This part of the layout is the most critical for performance and emissions. Time should be taken to carefully route these traces by hand.

The choice of magnetics will influence the routing of the transmit and receive lines. Mitel recommend the Valor Electronics ST6114 100Mb/s magnetics, however other magnetics can be used and will influence the transmit and receive traces. Both transmit and receive traces should be physically as short as possible with the minimum number of vias and corners. Where there is a trade off between transmit and receive paths the most sensitive path to consider is the receive path to the NWK914.

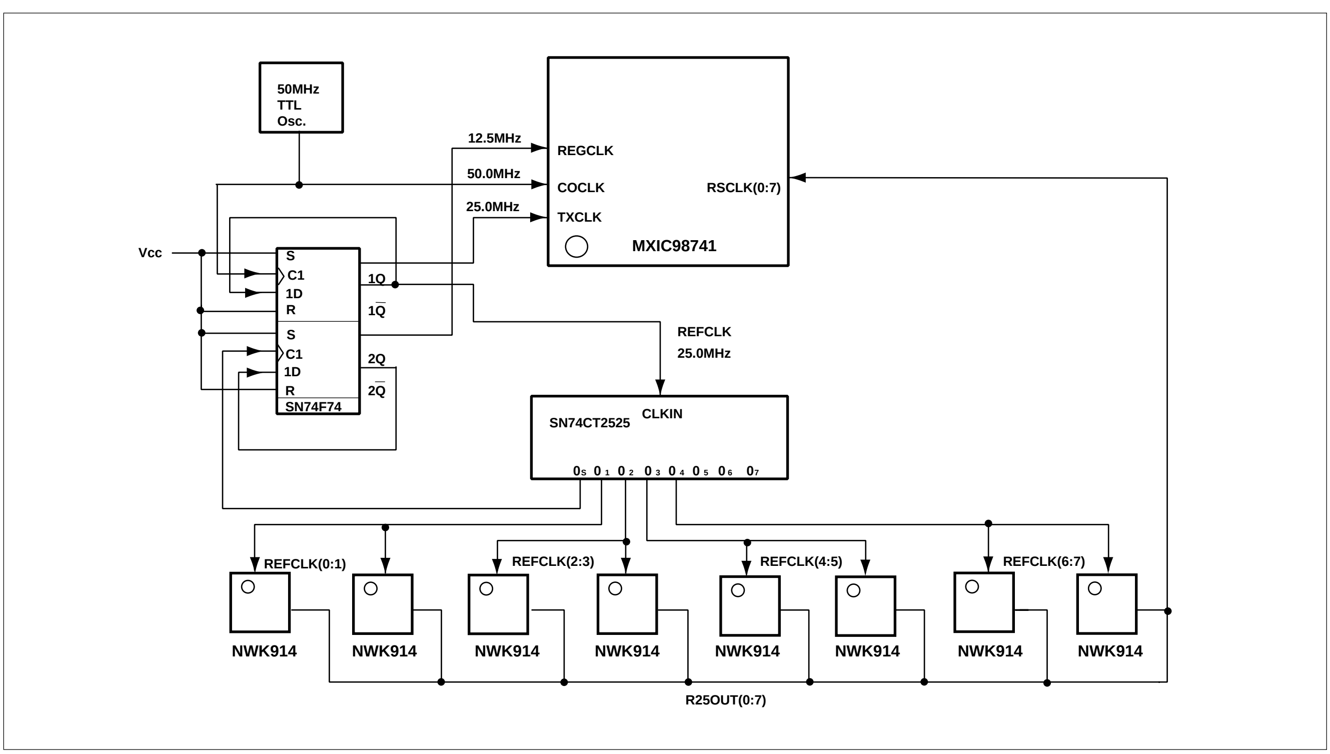


Fig.2 Clock distribution

The most important consideration is the distance between the receive resistors on pins 15 and 16 of the NWK914. This should be minimised as the received signal is most sensitive to any noise prior to entering the NWK914. Noise can be generated from the voltage supplies, mutual inductance from the magnetics etc.

3.2 NWK914 to RIC

At this stage in the design all signal levels are now relatively low speed at 25MHz and have a high noise immunity due to being 5V TTL. However it is still necessary to route clocks with care to avoid skew, noise and potential crosstalk. It is recommended that at least 0.05inch is left between any clocks and adjacent data lines where practical. All clock and data lines should be as short as possible to ensure common characteristics.

3.3 Phase Lock Loop Components

It is important to ensure that the Phase Lock Loop filter components are place as close to the device as possible and with no vias. This minimises any stray capacitance and noise that could effect the PLL characteristics.

3.4 Decoupling

We recommend that the power supply is split into five separate groupings as illustrated in Fig.3.

It is important to keep the TTL V_{CC} as clean as possible with electrolytic capacitors to ensure that spikes are not induced on to the main supply plane. Designs will fail if electrolytic capacitors are not used on this supply.

The receiver Phase Lock Loop (PLL) requires a separate supply through a ferrite bead as specified. This is to ensure that that sensitive circuits do not have any noise coupled into them, or produce any high frequency noise that could couple on to the main supply.

Mitel use Fig.3 as a reference for the recommended decoupling scheme. However this can be optimised by the systems vendor when a consideration of board space, performance and costs are relevant.

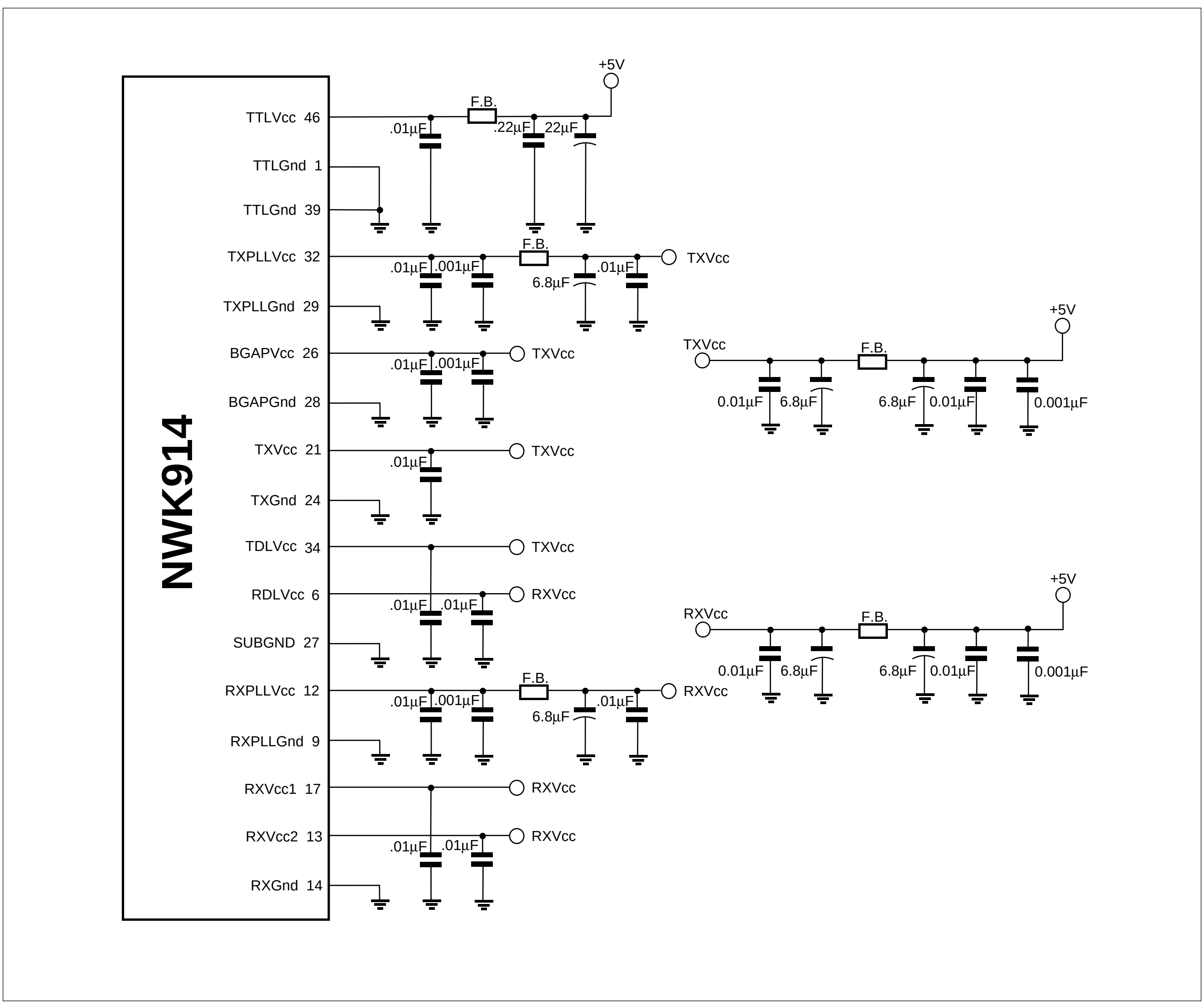


Fig.3 NWK914 decoupling arrangements

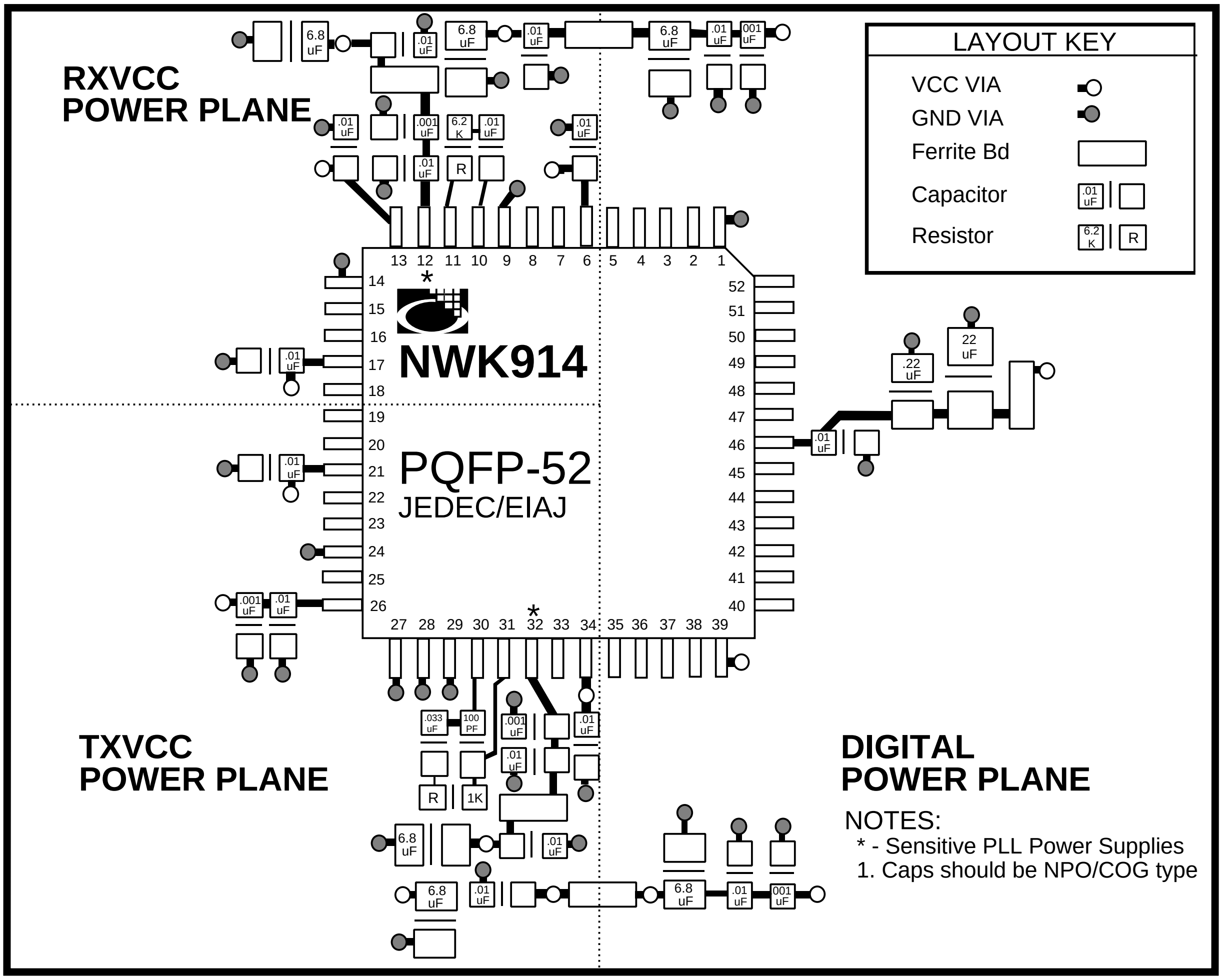


Fig.4 NWK914 recommended power planes

3.5 Power Supply and Ground Planes

The receiver logic requires a separate power plane under the NWK914 (as illustrated in Fig.4) to remove any potential noise in the receiver supply and to separate it from the transmit logic which could induce crosstalk. The ferrite bead isolates the receiver suppy from the main +5V supply plane.

The transmitter PLL requires the same decoupling arrangement as the receiver PLL through a separate ferrite bead.

The transmitter logic requires the same arrangement as the receiver logic, with a separate plane to avoid crosstalk.

Successful designs have used solid ground planes and also split ground planes that mirror the defined power planes above with narrow restrictions that connect to the main ground. The choice of grounding configuration is application dependent. In this application Mitel recommend a solid ground plane with the exception of voids at either side of each NWK914. This is a preventative measure to minimise currents crossing from one NWK914 to the other and inducing noise. See Figs.5 and 6.

It should be noted that this void should be mirrored similarly in the power supply plane . Another consideration is that there should be a void of power and ground under the magnetics to minimise cross talk. Refer to Figs.5 and 6.

References

1 Mitel Semiconductor NWK914 Data sheet DS4046
2 Macronix MX98741 Data sheet
3 National Semiconductor CGS74CT2525 Data sheet
4 Texas Instruments SN74F74 Data sheet
5 IEEE 802.3u 100Base-TX Specification
6 ANSI X3.263-1995

Magnetics Manufacturers

ST6114
Valor Electronics, Inc.
9715 Business Park Ave.
San Diego, CA 92131

PE68517
Pulse Engineering
PO Box 12235
San Diego CA 92112

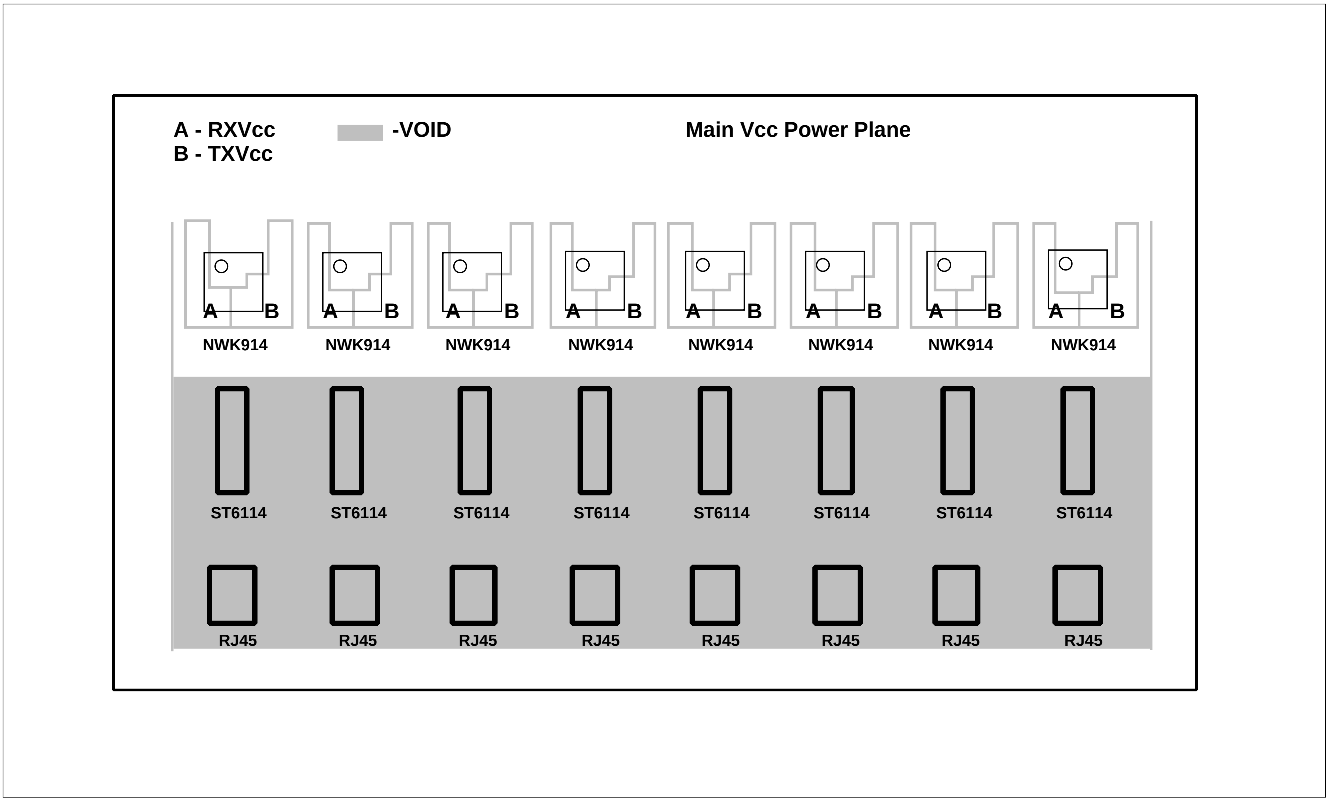


Fig.5 Suggested voids on V_{CC} plane

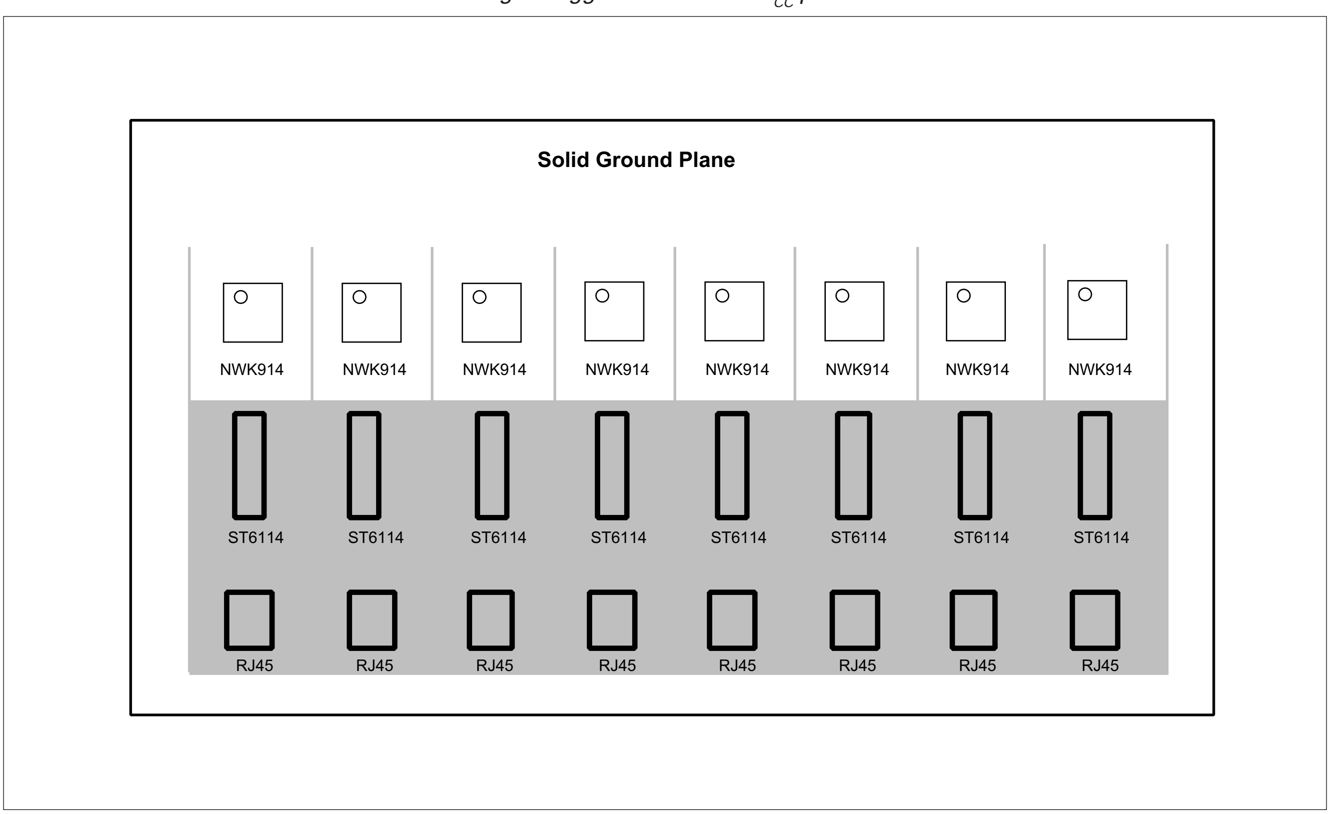


Fig.6 Suggested voids on GND plane

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